

**IN THE UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION**

BIAx CORPORATION,)
)
Plaintiff) Civil Action No. 2-05CV-184 (TJW)
v)
)
INTEL CORPORATION) JURY
)
and)
)
ANALOG DEVICES, INC.,)
)
Defendants/Counterclaimants.)

**DECLARATION OF LISA C. WARD IN SUPPORT OF INTEL'S OPPOSITION TO
BIAx'S MOTION TO AMEND ITS PRELIMINARY INFRINGEMENT
CONTENTIONS PURSUANT TO PATENT RULE 3-7**

I, Lisa C. Ward, declare as follows:

1. I am an attorney with the law firm of Orrick, Herrington & Sutcliffe LLP, counsel to defendant and counterclaimant Intel Corporation ("Intel"). I am a member of the State Bar of California. I make this declaration in support of Intel's Opposition to BIAx's Motion to Amend its Preliminary Infringement Contentions Pursuant to Patent Rule 3-7. I have personal knowledge of the facts set forth in this declaration and could and would competently testify under oath if called as a witness.

2. Attached hereto as Exhibit A is a true and correct copy of Robert McMillan, *Itanium 2 Montecito to be multithreaded*, ComputerWeekly.com (November 17, 2003) at <http://tinyurl.com/feusn>.

3. Attached hereto as Exhibit B is a true and correct copy of Rupert Goodwins, *Intel: Montecito or bust?*, ZDNet UK (September 9, 2004) at <http://tinyurl.com/l6jjd>.
4. Attached hereto as Exhibit C is a true and correct copy of Paul DeMone, *Sizing up the Super Heavyweights*, Real World Technologies (October 10, 2004) at <http://tinyurl.com/kfe6n>.
5. Attached hereto as Exhibit D is a true and correct copy of *Forthcoming Dual-Core Intel® Itanium® Processor Achieves Fastest Four-Way Floating Point Benchmark* (July 7, 2005) at www.intel.com/pressroom/archive/releases/20050707corp.htm.
6. Attached hereto as Exhibit E is a true and correct copy of *Intel® Itanium® 2 Processors Get Faster Bus Architecture* (July 18, 2005) at www.intel.com/pressroom/archive/releases/20050718comp.htm.
7. Attached hereto as Exhibit F is a true and correct copy of Jeffery Burt, *Multithreading Set for Processors*, eWeek.com (March 3, 2003) at <http://www.eweb.com/article2/0,1895,909993,00.asp>.
8. Attached hereto as Exhibit G is a true and correct copy of *Dual-Core Update to the Intel® Itanium® 2 Processor Reference Manual for Software Development and Optimization* (2006).
9. Attached hereto as Exhibit H is a true and correct copy of a letter from Caryl Arnese to Barry Graham dated 1/23/2006, producing document 75009DOC016622.

10. On February 21, 2006, Intel completed its production of the Montecito source code. Attached hereto as Exhibit I is a true and correct copy of a letter from Alex Chachkes to Edward Naidich dated 2/21/2006.

11. Attached hereto as Exhibit J is a true and correct copy of a letter from Edward Naidich to Alex Chachkes dated 5/2/2006.

12. Attached hereto as Exhibit K is a true and correct copy of Eastern District of Texas General Order 06-6 (February 27, 2006).

13. Attached hereto as Exhibit L is a true and correct copy of *The Microarchitecture of the Pentium 4 Processor*, Intel Technology Journal Vol. 5, Issue 1, February, 2001.

14. Attached hereto as Exhibit M is a true and correct copy of *Intel® Itanium® 2 Processor Reference Manual for Software Development and Optimization* (2004).

15. Attached hereto as Exhibit N is a true and correct copy of *Intel® Itanium™ Architecture Assembly Language Reference Guide* (2001).

16. Attached hereto as Exhibit O is a true and correct copy of the Court's Docket Control Order of December 21, 2005.

17. Attached hereto as Exhibit P is a true and correct copy of Marsha Eng, et. al, *Mesocode: Optimizations for Improving Fetch Bandwidth of Itanium Processors*, Workshop on Complexity-Effective Design (WCED) (May 2002).

18. Attached hereto as Exhibit Q is a true and correct copy of *Intel® Itanium® 2 Processor Hardware Developer's Manual* (2002).

19. Attached hereto as Exhibit R is a true and correct copy of Deborah T. Marr, et al,
Hyper-Threading Technology Architecture and Microarchitecture (2002).

Executed on June 8, 2006, at Irvine, California.

I declare under penalty of perjury under the laws of the United States of America that the foregoing is true and correct.


Lisa C. Ward